

Array Voltage

Source-circuit configuration is arguably the most important aspect of PV system design. The electrical and mechanical characteristics of a PV array follow from this fundamental design decision, which has a bearing on both labor and material costs. In addition, source-circuit configuration impacts system performance, in some cases negatively. Low dc array voltage, for example, is a common cause of substandard performance that occurs when open-circuit or operating voltages for an array persistently fail to meet minimum inverter dc input voltage thresholds over time. In this situation, the system design does not take into account the cumulative effects of a variety of real-world circumstances, including high ac grid voltage, array degradation, module-to-module voltage tolerance and high ambient temperatures. Fortunately, low dc array voltage is avoidable.

In this article, I detail array design best practices for determining the maximum number of modules in a source circuit. My approach is slightly less conservative than the industry standard and is supported by changes to the *National Electrical Code* that are introduced in the 2011 cycle. I also present recommendations for determining the minimum number of modules per source circuit. While these may be more conservative than current design standards, my opinions are based on years of experience. They are not influenced by the desire to sell more or less of any specific product but rather by the general desire to propagate well-designed PV systems that perform optimally for decades.

CONSIDER THE SOURCE

Interestingly enough, over the past decade inverter manufacturers have been the primary source of education regarding array design and source-circuit sizing. With all due respect, these companies usually have expertise in power electronics and not necessarily in PV array design. However, since the advent of the first string-sizing program—which was developed by John Berdner while he was the president of SMA America—it has become the industry standard for inverter manufacturers to provide PV array configuration advice.

The main drawback to having inverter manufacturers dictate array design is that they have a conflict of interest. Manufacturers want their products to be used as often as possible, and this is facilitated in part by allowing the maximum number of module configurations. In addition, although most manufacturers have stern warnings about exceeding the maximum inverter input voltage, they generally have little to say about circumstances where there is too little voltage for the inverter to fully operate the PV array.

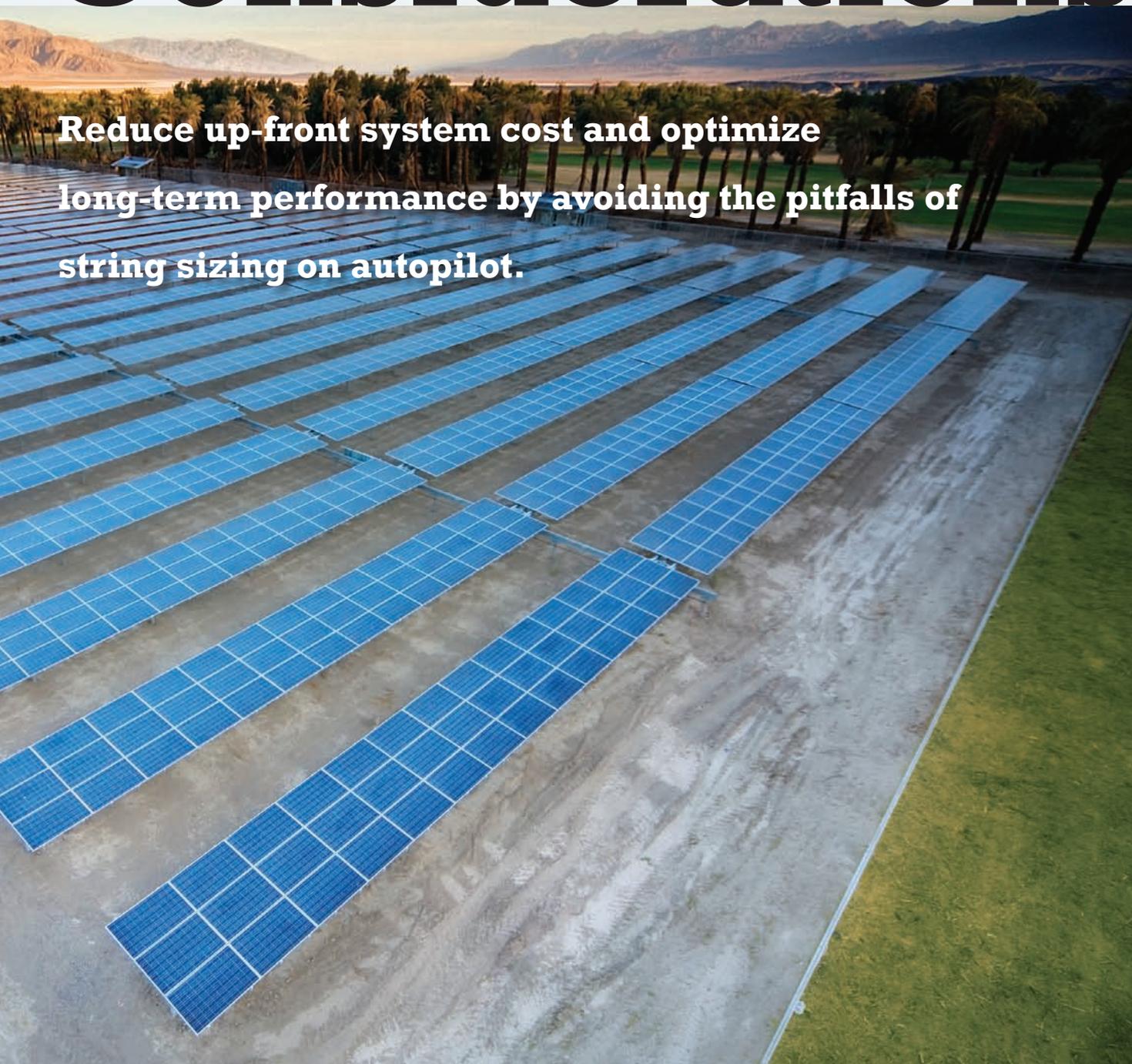
This skewed perspective informs both the string-sizing tools and the training materials that inverter manufacturers develop. The upshot is that inverters in the field seldom have a problem with high array voltage but routinely have problems with low array voltage. While low array voltage will not damage the inverter, it will compromise system performance.



By Bill Brooks, PE

Considerations

Reduce up-front system cost and optimize long-term performance by avoiding the pitfalls of string sizing on autopilot.



Courtesy SFG Solar and Xanterra Parks & Resorts

If the inverter cannot operate the array at its MPP, for example, then power production and energy harvest suffer. Problems can also result from open-circuit voltage being too low. On hot days, an array's V_{oc} can pass below the restart voltage of the inverter. The consequence is that if the inverter shuts down in the middle of the day due to a utility disturbance, it will not restart until the late afternoon when the V_{oc} increases. This can reduce the system's operating availability by several percentage points annually if utility disturbances are common in the summer, such as when utilities switch in distribution capacitors around noon on hot days to accommodate high air conditioning loads. To design a PV array that is well-matched to an inverter's operating window, system designers need to pay attention to the low end of the inverter operating voltage range, as well as to the maximum voltage allowed.

HIGH DC VOLTAGE

The maximum dc voltage for an inverter is clearly stated on the product specification sheet, installation manual or in tables, such as the one on pages 46–57. While relevant UL standards and *NEC* requirements certainly apply, the maximum voltage is generally set by the input capacitors and the ratings of the transistors in the inverter, so it is a constant rather than a variable limit.

Because it is possible to create overvoltage in an inverter by putting too many modules in series, some manufacturers keep the maximum dc input voltage in nonvolatile memory for warranty purposes. This allows the manufacturer's service technicians to verify the maximum dc voltage input to any inverter that is returned from the field under warranty. If the inverter was exposed to overvoltage conditions, then the manufacturer may choose not to provide a free replacement inverter. Historically, the most common cause of overvoltage is putting two source circuits in series rather than in parallel. This is a relatively easy mistake to make, especially in a small system with only two source circuits. Failure to properly account for low ambient temperatures is another potential cause of inverter overvoltage.

Some inverter manufacturers have claimed in their trainings that a 600 Vdc inverter will spontaneously combust if the array reaches 601 Vdc. While the inverter warranty may be voided if the array goes above the published maximum voltage, it is inconceivable that the capacitor or transistor tolerances are tight enough for the devices to operate well at 600 Vdc and explode at 601 Vdc. If that were true, inverters would also explode at 580 Vdc and they (usually) do not—at least not because of component tolerance.

Low temperature calculation. Most inverter manufacturers recommend using the site's record low temperature to determine the maximum number of modules per source circuit. While the record low temperature is easily attainable (see

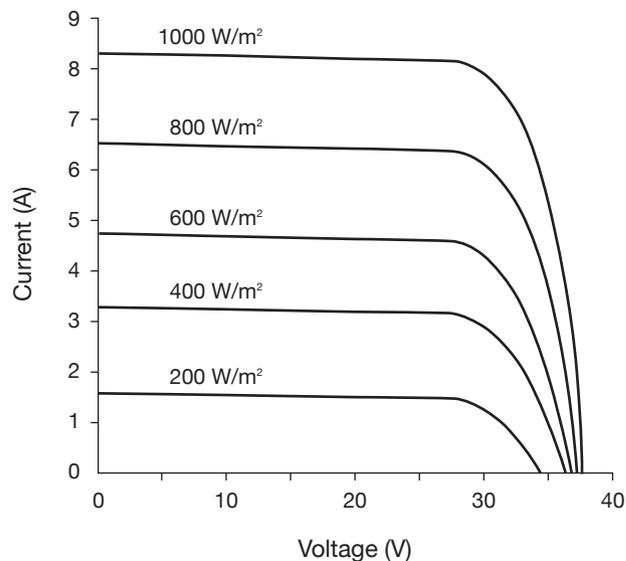


Figure 1 This representative module I-V curve is based on published curves for Yingli polycrystalline modules. It assumes a 25°C cell temperature and illustrates how open-circuit voltage responds to decreasing irradiance.

“Low Design Temperature,” p. 72), it is also overly conservative for maximum voltage calculations. The record low temperature is usually too conservative for design calculations because temperature is only one of two major factors that impact array open-circuit voltage. The other major factor is irradiance. As an example, look at the set of I-V curves in Figure 1, which assumes constant cell temperature and variable irradiance, and notice where the I-V curves intersect the horizontal axis. As irradiance decreases, so does open-circuit voltage.

The *NEC*, however, uses temperature only to determine maximum system voltage. The criterion for determining the maximum PV system voltage, according to Article 690.7(A), is to correct the source circuit open-circuit voltage for the “lowest expected ambient temperature.” Prior to the 2011 cycle, the *NEC* did not define the term *lowest expected ambient temperature*. However, the 2011 *NEC* will define it in an Informational Note (formerly known as a Fine Print Note) as follows: “One source for statistically valid, lowest expected ambient temperature design data for various locations is the Extreme Annual Mean Minimum Design Dry Bulb Temperature found in the American Society of Heating, Refrigeration, and Air Conditioning Engineers’ *ASHRAE Handbook—Fundamentals*. These temperature data can be used to calculate maximum voltage using the manufacturer’s temperature coefficients relative to the rating temperature of 25°C.”

An Informational Note is not a *Code* requirement and cannot be interpreted as such. System

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designers can use any authoritative source of data for the lowest expected ambient temperature. However, this Note is intended to help the designer and the AHJ focus on the most appropriate data for balanced array design. Since many system designers may not have ready access to the *ASHRAE Handbook*, the Extreme Annual Mean Minimum Design Dry Bulb Temperature data—hereafter referred to as the ASHRAE low design temperature data—is included in Appendix E of the *Expedited Permit Process for PV Systems* document that I wrote for the Solar America Board for Codes and Standards (Solar ABCs). This document is readily available on the SolarABCs website (see Resources) and includes data for more than 650 cities in the US.

Some may ask why ASHRAE data is better to use than the record low temperature. One reason is that using the record low temperature sometimes excludes acceptable source-circuit configurations that may in fact be preferred over shorter source circuits. (This is illustrated in “Case Study: Example dc Voltage Calculations,” p. 75.) In addition, the extra margin of safety that the record low temperature design provides is often statistically insignificant when compared to the ASHRAE design.

System designers must consider three important issues when determining an appropriate design temperature. First, statistically, the record low temperature may never occur again. Second, lower irradiance conditions in winter make it even less

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likely that peak irradiance ($1,000 \text{ W/m}^2$) will accompany the record low temperature, which is a necessary coincidence to achieve the calculated maximum voltage based on temperature. Third, to achieve in the field the maximum voltage that is possible on paper, the PV array must be in a condition that is as good as new. The modules cannot be soiled, mismatched or degraded; the maximum voltage for each of the installed modules must equal its published rating. The statistical likelihood of these conditions occurring at the same time is low.

The ASHRAE data provide statistically derived expected low temperatures. Although ASHRAE processes National Weather Service data for use by engineers sizing heating and cooling equipment, the data are also relevant to many other fields, including the electrical industry. The ASHRAE low design temperature data is derived by averaging the annual low temperature for every year on record. The result is a low temperature that has a 50% chance of occurring once a year at a specific location. Statistically, 50% of the years that a PV system is in service, the low for the year will be colder than this value—and for the other 50%, the low will never reach this value.

This does not mean that there is a 50:50 chance that the maximum voltage to the inverter will be exceeded in a given year. Remember that peak irradiance must

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Low Design Temperature

To find the record low temperature for any location in the US, go to Weather.com’s Monthly Climatology web page at the following URL and specify the desired zip code: weather.com/weather/climatology/monthly/zipcode.

For design purposes, however, a location’s record low temperature is very conservative, generally lower than the minimum expected ambient temperature at peak irradiance. The Extreme Annual Mean Minimum Design Dry Bulb Temperature data published by ASHRAE generally provide better low temperature design data in terms of statistical validity. These data are included in Appendix E of the *Expedited Permit Process for PV Systems*, which is available at the website for the Solar America Board for Codes and Standards.

One note of caution, however: All generalizations have exceptions. For example, a steeply tilted PV array in a high-altitude location subjected to snow reflectance may experience extreme open-circuit voltage conditions that even record low temperature design calculations will underestimate. ●



Proceed with caution While the Extreme Annual Mean Minimum Design Dry Bulb Temperature data published by ASHRAE are generally statistically valid for maximum array Voc calculations, more conservative data may be required for PV arrays in higher-altitude locations.

Low Array Voltage

The set of I-V curves in Figure 2 assumes source circuits of 14 Evergreen ES-195 modules, with 20 circuits connected in parallel to a Satcon PVS-50 inverter with a 305 Vdc minimum MPPT voltage. The ASHRAE low design temperature is 0°C, and the ASHRAE 2% design temperature is 45°C. The latter results in a minimum array operating voltage of 289.8 Vdc. (To see the underlying design calculations, refer to “Array to Inverter Matching,” December/January 2009, *SolarPro* magazine.)

As evidenced by the intersection of the dotted line and the I-V curve for the ASHRAE 2% design temperature, on the hottest days of summer when the solar resource is greatest, the inverter is unable to operate the array at its maximum power point. Any energy the inverter cannot harvest is money left on the table. This is clearly not an acceptable array design.

Adapting the design to 15 modules per source circuit gets the minimum array operating voltage up to 310.5 Vdc, which is higher than the minimum inverter MPPT voltage. However, this does not provide adequate margin to account for the cumulative effects of high ac grid voltage, array degradation or voltage mismatch. The best array design is actually 16 modules per source circuit, which results in a minimum array operating voltage of 331.2 Vdc, before any other derates are applied, and a maximum open-circuit voltage of 571.2 Vdc. ●

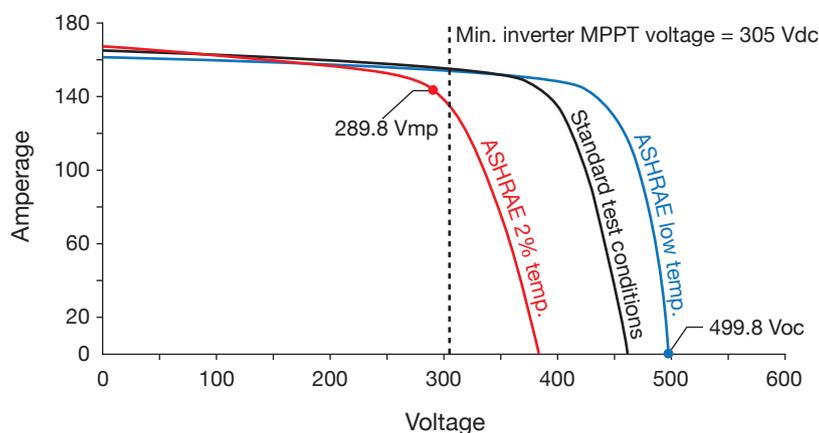


Figure 2 With only 14 modules in series, the maximum power point for the I-V curve in red occurs below the inverter’s minimum MPPT voltage.

accompany this temperature, and the modules must perform as if they were new and perfectly matched. Ultimately, engineering design involves a series of decisions based on the likelihood of an occurrence and the consequences should the worst case happen. Good system engineering balances valid concerns to develop a design that keeps all the equipment operating properly within acceptable limits. Using the record low temperature does not eliminate the statistical possibility of exceeding an inverter’s maximum input voltage; it simply lowers the possibility relative to a higher temperature. I recommend using the ASHRAE low design temperature data unless there is a specific need for more conservative design data.

when the array dc voltage is at its lowest level due to the high ambient temperatures. While 5% higher ac voltage is unusual, 2–3% higher voltage is common on hot days, since utilities raise voltage to enable them to run more power through their distribution circuits to satisfy air conditioning loads.

Array degradation. System designers must be aware that the minimum voltage from a PV module, and thus an array, changes over time. All PV arrays degrade in power, both in voltage and current. At a minimum, designers should factor in an annual power loss of 0.5%.

Since no conclusive data exists regarding how much of this loss is expressed in voltage versus current, a reasonable

LOW DC VOLTAGE

Inverter specification sheets seem simple enough to use, but some knowledge of how inverters work is required to interpret them. For example, in contrast to an inverter’s published high dc voltage limit, the low dc voltage limit for most inverters is a variable that changes in response to the grid voltage. In addition, the voltage that an array is capable of, given specific environmental conditions like irradiance and cell temperature, diminishes over time. Designers must also account for the effects of module voltage tolerance when performing acceptable low dc voltage calculations. Many of the most egregious PV source-circuit design mistakes are due to a failure to account for these combined factors; these designs result in array voltages that are too low for the inverter.

High ac grid voltage. While a manufacturer might state that the low dc voltage for its inverter is 330 Vdc, this is usually the lowest acceptable dc input voltage at the nominal grid voltage. For residential systems, the nominal single-phase voltage is 240 Vac; for larger systems, the nominal 3-phase voltage might be 208, 240 or 480 Vac. As the ac voltage varies above nominal, the minimum dc input voltage rises as well.

If the ac voltage rises 5%, which is possible on hot summer afternoons, the minimum dc voltage also rises 5%. Therefore, an inverter with a minimum voltage rating of 330 Vdc has a minimum voltage of 347 Vdc under those 5% higher ac voltage conditions. This condition often occurs at precisely the time

design decision is to equally allocate the loss between current and voltage. This means that a typical array should be designed with the understanding that it will lose 0.25% or more of its voltage each year. Over 25 years, a minimum loss to calculate would be about 6% ($0.9975^{25} = 0.939$).

Voltage tolerance. While PV modules may have relatively tight power tolerances (averaging about +3%/-3%), the voltage and current tolerances are typically much larger—perhaps as large as +10%/-10%. This uncertainty is difficult to plan for in design. If a module is relatively low in voltage, its power specification is met by having an offsetting high current, because power is the product of volts times amps. Given the lack of information on module voltage tolerance available, it is best to err on the side of caution and assume an extra 5% dc voltage loss in the array.

Combined impacts. To arrive at an optimal minimum dc voltage for the array, add the effects of all the issues together. Currently, string-sizing programs calculate the minimum voltage based on the temperature-adjusted maximum power voltage of the module. If the high ac voltage accounts for 3%, array degradation for 6%, and module voltage tolerance for 5%, then the array should be designed to operate with a voltage that is at least 14% higher than the temperature-adjusted maximum power voltage for a given location.

The way to avoid problems associated with low dc voltage is to increase the array voltage. When using string-sizing programs, the simple rule I recommend is to eliminate the lowest voltage option—the source circuit with the least number of modules in series. If possible, throw away the two shortest source-circuit options. For example, if the sizing program allows 12, 13, 14 or 15 modules in series, limit the choices to 14 or 15 modules.

While this approach may work well in general, it is important for system designers to perform detailed low dc voltage calculations for specific array configurations. Designers should use the highest expected continuous ambient temperature for calculation purposes. According to the Copper Development Association, the highest ASHRAE temperature data that is likely to create a 3-hour continuous condition, per the definition of *continuous* found in *NEC* Article 100, is the 2% Annual Design Dry Bulb Temperature, which is also found in Appendix E of the *Expedited Permit Process for PV Systems*. For designers who feel that the ASHRAE 2% temperature is not high enough, the same table also includes ASHRAE Extreme Annual Mean *Maximum* Design Dry Bulb Temperature data, which can be used for even more conservative voltage or ampacity calculations.

CASE STUDY: EXAMPLE DC VOLTAGE CALCULATIONS

This case study illustrates how to implement the high and low dc voltage recommendations described in this article. It assumes a 50 kW inverter because designers working on smaller

arrays, especially those under 10 kW, can be heavily influenced by a desire to fully exploit the available inverter capacity. This often leads to array voltage compromises that are unnecessary in larger systems. The inverter in this case is large enough that its capacity does not drive array voltage design. The relevant design details for this case study are as follows.

Location: Raleigh, NC

Low design temperature: -13°C, per ASHRAE Extreme Annual Mean Minimum Design Dry Bulb Temperature

Record low temperature: -21°C, per Weather.com

High design temperature: 34°C, per ASHRAE 2% Annual Design Dry Bulb Temperature

PV module: Yingli YL230P-29b, 230 W STC, 29.5 V_{mp}, 7.8 I_{mp}, 37.0 V_{oc}, 8.4 I_{sc}, -0.137 V/°C temperature coefficient of V_{oc} (-0.37%/°C x 37.0 V_{oc}), -0.133 V/°C temperature coefficient of V_{mp} (based on the published temperature coefficient for P_{mp}, -0.45%/°C x 29.5 V_{mp})

Inverter: Satcon PVS-50, 50 kW, 600 V_{dc} maximum input, 305–600 V_{dc} MPPT range

Maximum modules in series. To determine the maximum number of modules in series, first calculate the per-module maximum voltage as follows:

$$V_{MAX} = V_{OC} + ((T_{LOW} - T_{REF}) \times \alpha V_{OC})$$

where T_{LOW} is the ASHRAE Extreme Annual Mean Minimum Design Dry Bulb Temperature; T_{REF} is the cell temperature at STC; and αV_{OC} is the temperature coefficient of V_{oc}.

$$\begin{aligned} V_{MAX} &= 37.0 \text{ V} + ((-13^\circ\text{C} - 25^\circ\text{C}) \times -0.137 \text{ V}/^\circ\text{C}) \\ &= 37.0 \text{ V} + (-38^\circ\text{C} \times -0.137 \text{ V}/^\circ\text{C}) \\ &= 37.0 \text{ V} + 5.2 \text{ V} \\ &= 42.2 \text{ V} \end{aligned}$$

Divide the maximum inverter input voltage by the temperature-corrected open-circuit voltage and round down to the nearest whole number to determine the maximum number of modules in series:

$$\begin{aligned} N_{MAX} &= 600 \text{ Vdc} / 42.2 \text{ V} = 14.2 \\ &= 14 \text{ modules in series} \end{aligned}$$

Minimum modules in series. To determine the minimum number of modules in series, first calculate the per module minimum voltage as follows:

$$V_{MIN} = (V_{MP} + ((T_{HI} + T_{RISE} - T_{REF}) \times \beta V_{MP}))$$

where T_{HI} is the ASHRAE 2% Annual Design Dry Bulb Temperature, T_{RISE} is the rise in cell temperature expected

considering array mounting (typically 20°C to 30°C), and βV_{MP} is the temperature coefficient of V_{mp}.

$$\begin{aligned} V_{MIN} &= 29.5 \text{ V} + ((34^\circ\text{C} + 20^\circ\text{C} - 25^\circ\text{C}) \times -0.133 \text{ V}/^\circ\text{C}) \\ &= 29.5 \text{ V} + (29^\circ\text{C} \times -0.133 \text{ V}/^\circ\text{C}) \\ &= 29.5 \text{ V} - 3.9 \text{ V} \\ &= 25.6 \text{ V} \end{aligned}$$

Select and apply a multiplier to account for the combined effects of high ac grid voltage, array degradation and module voltage tolerance. 0.85 is used in this case:

$$\begin{aligned} V_{MIN} &= 25.6 \text{ V} \times 0.85 \\ &= 21.8 \text{ V} \end{aligned}$$

Divide the minimum MPPT voltage by the minimum voltage per module and round up to the nearest whole number to determine the minimum number of modules in series:

$$\begin{aligned} N_{MIN} &= 305 \text{ V} / 21.8 \text{ V} = 13.99 \\ &= 14 \text{ module in series} \end{aligned}$$

Comparison of results. It is now possible to recalculate the acceptable source-circuit configurations using standard assumptions for a string-sizing program. There are two main differences in the calculations.

First, use the record low temperature for the location in place of the ASHRAE Extreme Annual Mean Minimum Design Dry Bulb Temperature for the V_{MAX} and N_{MAX} calculations:

$$\begin{aligned} V_{MAX} &= 37.0 \text{ V} + ((-21^\circ\text{C} - 25^\circ\text{C}) \times -0.137 \text{ V}/^\circ\text{C}) \\ &= 37.0 \text{ V} + (-46^\circ\text{C} \times -0.137 \text{ V}/^\circ\text{C}) \\ &= 37.0 \text{ V} + 6.3 \text{ V} \\ &= 43.3 \text{ V} \end{aligned}$$

$$\begin{aligned} N_{MAX} &= 600 \text{ Vdc} / 43.3 \text{ V} = 13.9 \\ &= 13 \text{ modules in series} \end{aligned}$$

Second, do not apply a 0.85 multiplier as part of the V_{MIN} calculations. This means that the minimum number of modules per source circuit is calculated using a V_{mp} of 25.6 V_{dc}:

$$\begin{aligned} N_{MIN} &= 305 \text{ V} / 25.6 \text{ V} = 11.9 \\ &= 12 \text{ module in series} \end{aligned}$$

The best array design for this case study calls for 14 modules per source circuit. However, the simplest string-sizing program specifies 12 to 13 modules per source circuit. More sophisticated string-sizing programs apply a margin of safety to the minimum expected dc voltage to account for high ac grid voltage, array degradation and module-to-module voltage mismatch. Using PVSelect.com, for

example, to calculate the acceptable string sizes for this case study disqualifies source circuits of 12 modules. However, if the designer is not using ASHRAE low design temperature data, even PVSelect.com cannot identify the best design option. Assuring the best design requires both accurate calculations and proper data.

SIZING THINGS UP

I am not suggesting that inverter manufacturers do not provide a valuable service with their string-sizing tools. Without these resources, the number of array design mistakes would undoubtedly be many times what it is today. Nevertheless, system designers routinely make mistakes, in spite of the fact that they have ready access to many easy-to-use string-sizing tools. The results of the low voltage mistakes described here are not dangerous; they do not pose a hazard to persons or property; they do not violate *Code*. They simply miss the mark of reducing up-front system cost and optimizing long-term performance. Designers need to keep in mind that all “approved” string sizes are not created equal.

From an installed cost point of view, it is always better to put the maximum number of modules in series. This delivers the greatest amount of power per pair of source-circuit

conductors. Longer strings also increase the array voltage, which has voltage drop benefits when cables are sized. Getting the array voltage up also provides insurance when it is needed most against insidious low dc voltage problems that result in poor system performance precisely when the solar resource is greatest. On 5 kW or 50 kW net-metered projects, the difference in performance between having 14 modules in series or 12 or 13 modules in series might not register with the customer. However, on 500 kW or 5 MW projects that are PPA financed, this will make a world of difference in both the installed costs and the revenue generated over the life of the systems. ⊕

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Resources

American Society of Heating, Refrigeration, and Air-Conditioning Engineers / ashrae.org

Blue Oak PV Selection Tool / pvselect.com

Solar America Board for Codes and Standards (Solar ABCs) / solarabcs.org/permitting